



SHEET 1 OF 4

FORM PTO - 1449

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-044C1

APPLICANT(S): Fitzgerald *et al.*

SERIAL NO.: 10/611,739

FILING DATE: July 1, 2003

GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Dle	A166	2002/0063292	05/30/2002	Armstrong <i>et al.</i>			
	A167	2002/0190284	12/19/2002	Murthy <i>et al.</i>			12/30/1999
	A168	2004/0007724	01/15/2004	Murthy <i>et al.</i>			07/12/2002
	A169	2004/0014276	01/22/2004	Murthy <i>et al.</i>			07/16/2002
	A170	2004/0070035	04/15/2004	Murthy <i>et al.</i>			07/23/2003
	A171	2004/0084735	05/06/2004	Murthy <i>et al.</i>			07/23/2003
	A172	2004/0119101	06/24/2004	Schrom <i>et al.</i>			12/23/2002
	A173	2004/0142545	07/22/2004	Ngo <i>et al.</i>			01/17/2003
	A174	2004/0173815	09/09/2004	Yeo <i>et al.</i>			03/04/2003
	A175	5,089,872	02/18/1992	Ozturk <i>et al.</i>			
	A176	5,242,847	09/07/1993	Ozturk <i>et al.</i>			
	A177	6,228,694	05/08/2001	Doyle <i>et al.</i>			
	A178	6,235,568	05/22/2001	Murthy <i>et al.</i>			
	A179	6,281,532	08/28/2001	Doyle <i>et al.</i>			
	A180	6,326,664	12/04/2001	Chau <i>et al.</i>			
	A181	6,563,152	05/13/2003	Roberds <i>et al.</i>			12/29/2000
	A182	6,605,498	08/12/2003	Murthy <i>et al.</i>			03/29/2002
	A183	6,621,131	09/16/2003	Murthy <i>et al.</i>			11/01/2001
	A184	6,657,223	12/02/2003	Wang <i>et al.</i>			10/29/2002
	A185	6,703,648	03/09/2004	Xiang <i>et al.</i>			10/29/2002
Dle	A186	6,743,684	06/01/2004	Liu			10/11/2002
EXAMINER Dle				DATE CONSIDERED 10/25/04			

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FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
<i>De</i>	C98	Gannavaram, <i>et al.</i> , "Low Temperature ($\leq 800^{\circ}\text{C}$) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2000), pp. 437-440.							
	C99	Ge <i>et al.</i> , "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003) pp. 73-76.							
	C100	Ghani <i>et al.</i> , "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003), 978-980.							
	C101	Hamada <i>et al.</i> , "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 4 (April 1991), pp. 895-900.							
	C102	Huang <i>et al.</i> , "Isolation Process Dependence of Channel Mobility in Thin-Film SOI Devices," <u>IEEE Electron Device Letters</u> , Vol. 17, No. 6 (June 1996), pp. 291-293.							
	C103	Huang <i>et al.</i> , "LOCOS-Induced Stress Effects on Thin-Film SOI Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 44, No. 4 (April 1997), pp. 646-650.							
	C104	Huang, <i>et al.</i> , "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain", <u>IEEE Electron Device Letters</u> , Vol. 21, No. 9, (Sept. 2000) pp. 448-450.							
<i>De</i>	C105	Iida <i>et al.</i> , "Thermal behavior of residual strain in silicon-on-insulator bonded wafer and effects on electron mobility," <u>Solid-State Electronics</u> , Vol. 43 (1999), pp. 1117-1120.							
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
<i>De</i>	C106	Ito <i>et al.</i> , "Mechanical Stress Effect on Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 247-250.							
	C107	Lochtefeld <i>et al.</i> , "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 12 (2001), pp. 591-593.							
	C108	Ootsuka <i>et al.</i> , "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 575-578.							
	C109	Ota <i>et al.</i> , "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2002), pp. 27-30.							
	C110	Öztürk, <i>et al.</i> , "Advanced Si _{1-x} Ge _x Source/Drain and Contact Technologies for Sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2002), pp. 375-378.							
	C111	Öztürk, <i>et al.</i> , "Ultra-Shallow Source/Drain Junctions for Nanoscale CMOS Using Selective Silicon-Germanium Technology," <u>Extended Abstracts of International Workshop on Junction Technology</u> , (2001), pp. 77-82.							
	C112	Öztürk, <i>et al.</i> , "Selective Silicon-Germanium Source/Drain Technology for Nanoscale CMOS," <u>Mat. Res. Soc. Symp. Proc.</u> , Vol. 717, (2002), pp. C4.1.1-C4.1.12.							
	C113	Öztürk, <i>et al.</i> , "Low Resistivity Nickel Germanosilicide Contacts to Ultra-Shallow Si _{1-x} Ge _x Source/Drain Junctions for Nanoscale CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> (2003), pp. 497-500.							
<i>De</i>	C114	Shimizu <i>et al.</i> , "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," <u>IEEE International Electron Devices Meeting Technical Digest</u> (2001), pp. 433-436.							
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
Dle	C115	Thompson <i>et al.</i> , "A Logic Nanotechnology Featuring Strained-Silicon," <u>IEEE Electron Device Letters</u> , Vol. 25, No. 4 (April 2004), pp. 191-193.							
	C116	Thompson <i>et al.</i> , "A 90 nm Logic Technology Featuring 50nm Strained-Silicon Channel Transistors, 7 layers of Cu Interconnects, Low k ILD, and 1um ² SRAM Cell," <u>IEEE International Electron Devices Meeting Technical Digest</u> (2002), pp. 61-64.							
	C117	Tiwari <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (1997), pp. 939-941.							
Dle	C118	Uchino, <i>et al.</i> , "A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-µm CMOS ULSIs," <u>IEEE International Electron Device Meeting Technical Digest</u> (1997), pp. 479-482.							
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